

VPX-1000S-3P-G-24V

1000W CONDUCTION-COOLED VITA 62 POWER SUPPLY

PULSE-LOAD READY

EXTERNAL 100 kHz OUTPUT-REGULATOR SYNC

DESIGNED & MANUFACTURED IN THE USA



VPX-1000S platform shown

Built for pulsed loads.

Stable +24V power for demanding mission systems

A rugged 1000W VITA 62 supply for repetitive pulsed loads. The +24V regulator can synchronize to a user clock for coordinated switching in radar, EW, RF and other mission systems.

1000W

TOTAL OUTPUT POWER

Conduction cooled

+24V

MAIN OUTPUT

Pulse-load configured

EXTERNAL SYNCHRONIZATION

100 kHz nominal, +/-1 kHz, 40-60% duty cycle
+3.3V TTL-compatible SYNC*/SYNC* RTN interface

LARGE CAPACITIVE-LOAD STARTUP

Supports startup into large capacitor banks while maintaining controlled +24V output

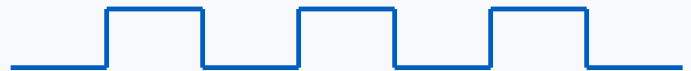
KEY FEATURES

- 1000W total output in a 6U x 5HP (1 inch) x 160mm modular design
- Three-phase 115/200Vac, 60Hz input with active power factor correction greater than 0.98
- Input current THD not exceeding 4%
- Meets MIL-STD-1399, section 300A (type 1) grounded for the voltage range specified
- VITA 62 output; +24V/41.7A
- 100 kHz external synchronization for coordinated system operation
- Custom input/output configurations available
- Conduction cooled through VITA 62 wedge-lock retainers
- N+1 redundant operation with internal ORing FETs/diodes
- Remote sense, current limit, overvoltage and overtemperature protection
- Rugged side-cover construction supports two-level military maintenance
- Optional parylene conformal coating and application-specific I/O configurations
- Designed and manufactured in the USA
- Greater than 150,000 hours MTBF
- One year warranty

WHY PULSE-LOAD CAPABILITY MATTERS

Radar transmitters, RF amplifiers, electronic-warfare equipment and other mission systems can demand fast, repetitive bursts of current. The VPX-1000S-3P-G-24V is configured around the customer's pulse profile to maintain controlled output voltage through these dynamic events.

Peak, width, repetition rate and duty cycle are application-specific



REPETITIVE PULSE / BURST LOAD PROFILE

APPLICATIONS

- Radar and phased-array subsystems
- Electronic warfare and RF payloads
- High-power communications systems
- Mission computing and sensor systems
- Directed-energy and high-power RF systems
- High-power sensor and surveillance systems

ELECTRICAL SPECIFICATIONS

Nominal Input	115/200Vac, 3-phase, 60Hz grounded
Operating Range	+20%, -15%; input transients +/-25%
Power Factor	Greater than 0.98 at full load
Input Current THD	4% maximum
Input Load Balance	Phase current within 5% of 3-phase average
Inrush Current	Less than 4ms; 40A at 200Vac
Hold-Up Time	20ms minimum after loss of AC input at full load
Efficiency	89% typical, configuration dependent
Turn-On Time	1 second maximum from power-up
Main Output	+24V nominal; up to 1000W total output
Capacitive-Load Startup	High-inrush startup into large capacitor banks
Line / Load Regulation	+/-2% over input range and 0-100% load
Ripple & Noise	0.5% maximum or 50mV, whichever is greater
Remote Sense	Compensates for up to 0.5V total distribution drop

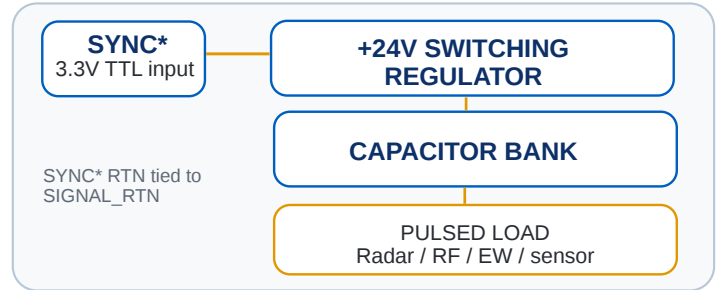
PROTECTION / CONTROLS

Current Limiting	Protected; automatic recovery after overload removal
Overvoltage	Shutdown at approximately 130% of nominal output
Overtemperature	Automatic shutdown; recycle input to reset
Reverse Voltage	Protected to the supply current rating
Enable* / INHIBIT*	VITA 62 compliant control interfaces
SYSRESET* / FAIL*	VITA 62 compliant status interfaces
I2C / Addressing	VITA 62 compliant management interface
Indicators	Green Input OK and red power-supply fault LEDs

MECHANICAL / ENVIRONMENTAL / QUALITY

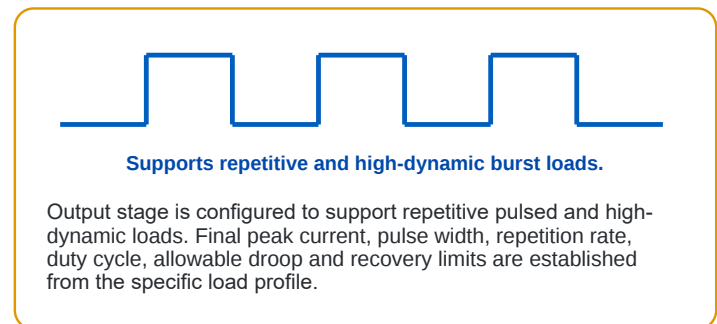
Cooling	Conduction cooled via wedge-lock retainers
Operating Temperature	-40C to +71C at wedge-lock edge, 1000W
Storage Temperature	-55C to +105C
Humidity	Up to 95% non-condensing
Size / Weight	6U x 5HP (1 inch) x 160mm; approximately 3.5 lb

EXTERNAL SYNCHRONIZATION



Input Pins	SYNC* / SYNC* RTN
Interface	+3.3V TTL-compatible, buffered by SN74LVC1G34
Frequency	100 kHz nominal, +/-1 kHz
Duty Cycle	40-60%
Return	SYNC* RTN tied to SIGNAL_RTN
Sync Stage	Only the +24V output switching regulator
Other Stages	Input/PFC stage and auxiliary output are not

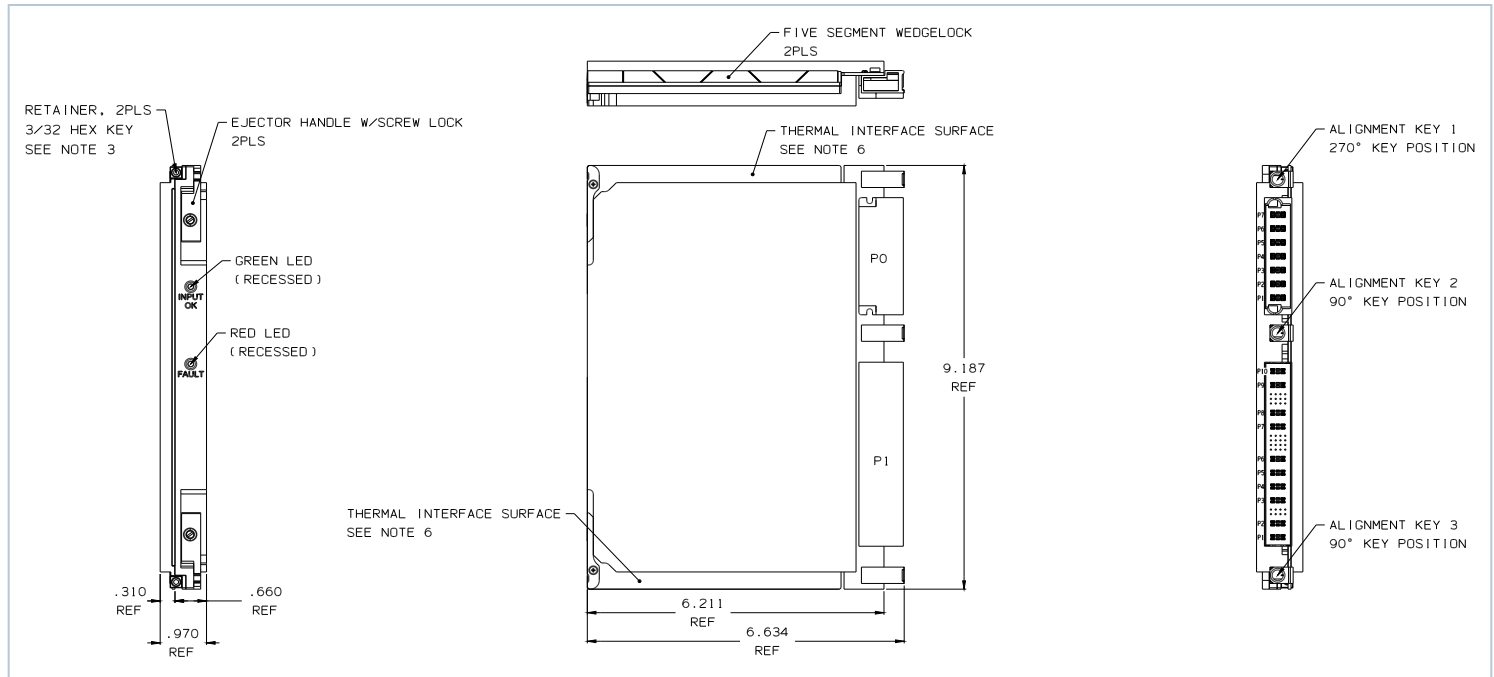
PULSED-LOAD CONFIGURATION



EMC	Designed to meet MIL-STD-461 with qualified external filtering
Environmental	Platform designed for MIL-STD-810 environments
Input Power	MIL-STD-1399, Section 300A platform heritage
Workmanship	IPC J-STD-001 Class 3 manufacturing
Manufacturing	Designed and manufactured by Switching Power, Inc. in New York, USA

NOTE: Pulse-load performance is application dependent. Peak current, pulse width, repetition rate, duty cycle, allowable voltage droop, and recovery requirements should be confirmed against the specific load profile and system requirements.

MECHANICAL OUTLINE



P0 - AC/DC INPUT CONNECTOR

TE CONNECTIVITY P/N 6450843-6

PIN NO.	SIGNAL
P7	PHASE A
P6	PHASE B
P5	PHASE C
P4	NEUTRAL
P3	N/C
P2	N/C
P1	CHASSIS GND

P1 - DC OUTPUT CONNECTOR

TE CONNECTIVITY P/N 6450849-6

PIN NO.	SIGNAL	PIN NO.	SIGNAL	PIN NO.	SIGNAL
P10	+24V/41.7A	B4	GA2*	C6	N/C
P9	+24V/41.7A	C4	GA1*	D6	SYSRESET*
A9	+24V SENSE	D4	GA0*	A5	GAP*
B9	+24V SENSE	A3	N/C	B5	GA4*
C9	N/C	B3	N/C	C5	SCLK
D9	SYNC*	C3	NED	B2	FAIL*
A8	+24V SENSE RTN	D3	NED_RTN	C2	INHIBIT*
B8	+24V SENSE RTN	P6	N/C	D2	ENABLE*
C8	N/C	P5	N/C	A1	N/C
D8	SYNC*_RTN	P4	N/C	B1	N/C
A7	N/C	P3	N/C	C1	N/C
B7	N/C	A2	N/C	D1	N/C
C7	N/C	P8	POWER RTN	P2	N/C
D7	SIGNAL_RTN	P7	POWER RTN	P1	POWER_RTN
D5	SDA	A6	N/C		
A4	GA3*	B6	N/C		

NOTES

1. VITA 62 COMPLIANT 6U POWER SUPPLY, CONDUCTION COOLED.
2. 1 INCH PITCH FORM FACTOR.
3. WEDGELOCK RETAINER INSTALLATION TORQUE VALUE IS 10 IN-LBS.
4. TOTAL POWER NOT TO EXCEED 1000 WATTS.

5. PRIMARY AND SECONDARY SIDE COVERS ARE 2 LEVEL MAINTENANCE COMPATIBLE.
6. OPERATING TEMPERATURE (AT THERMAL INTERFACE SURFACE): -40°C TO +85°C @ 1000W.
7. SYNC*/SYNC*_RTN IS AN INPUT TO A +3.3V TTL BUFFER PART NUMBER SN74LVC1G34. NOMINALLY 100 kHz +/-1 kHz, WITH A 40-60% DUTY CYCLE. SYNC*_RTN IS TIED TO SIGNAL_RTN.
8. ONLY THE OUTPUT +24V SWITCHING REGULATOR WILL BE SYNCHRONIZED TO THIS EXTERNAL CLOCK REFERENCE.